XTAG-2 Hardware Manual

Version 1.0

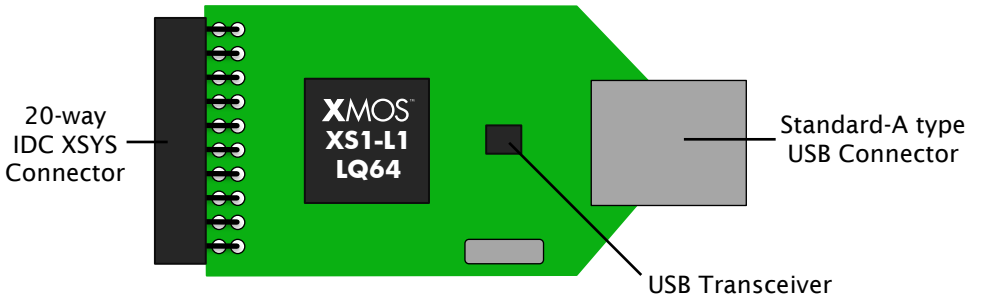
XMOS

Publication Date: 2009/09/23

1 Introduction

The XTAG-2 debug adapter converts between an XMOS XSYS connector and USB 2.0, providing pins for JTAG control, system reset, processor debug, one duplex UART link and one duplex serial XMOS Link. The XTAG-2 debug adapter can be used to connect XMOS development kits to most PCs, and provide a 5V power supply.

The diagram below shows the layout of the components on the card.



To debug a board with the XTAG-2 you must use the XMOS Design Tools version 9.9 or later, available from the XMOS web site.

2 XS1-L1 Device

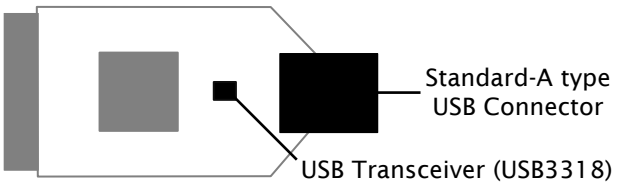
The XTAG-2 is based on a single XS1-L1 device in a 64LQFP package. The XS1-L1 consists of a single XCore, which comprises an event-driven multi-threaded processor with tightly integrated general purpose I/O pins and 64 KBytes of on-chip RAM. The pins are brought out of the package and connected to the card's components as follows:

- USB Connector
- XSYS 20-way IDC header (female)

The processor has ports that are directly connected to the I/O pins.

3 USB Connector

The XTAG-2 uses a Standard-A type USB connector to link to a PC.



The USB connector is connected to an SMSC USB3318 high-speed transceiver using a ULPI interface. The I/O pins for the USB transceiver are mapped to ports on the processor as described in the tables below.

Pin	Port		Processor
	4bit	8bit	
XD12	P1E0		ULPI_STP
XD13	P1F0		ULPI_NXT
XD14	P4C0	P8B0	ULPI_DATA[0:7]
XD15	P4C1	P8B1	
XD16	P4d0	P8B2	
XD17	P4D1	P8B3	
XD18	P4D2	P8B4	
XD19	P4D3	P8B5	
XD20	P4C2	P8B6	
XD21	P4C3	P8B7	
XD22	P1G0		ULPI_DIR
XD23	P1H0		ULPI_CLK

Each pin can be configured either as a 4-bit port or an 8-bit port. The configuration is determined by the set of port initialisers used in the software.

The reset pin on the USB transceiver is mapped to a 1-bit port on the processor as described below:

Pin	Port	Processor
XD24	P1I0	PHY_RST_N

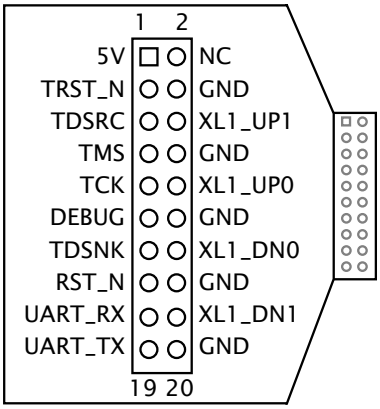
4 XSYS Connector

The XTAG-2 includes an XSYS 20-way IDC header, which can be used to connect it to an XMOS development board for debugging programs on the hardware.

The XSYS connector provides pins for JTAG control, system reset, processor debug, a duplex UART link and a 2-bit serial XMOS Link.

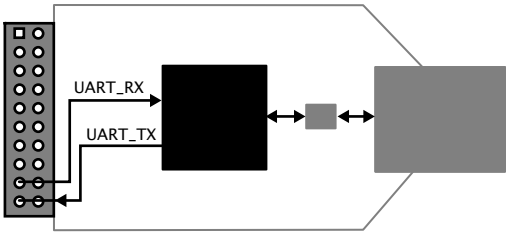
Pin	Signal	Direction	Description
1	5V	Target to Host	Power
2	NC	N/A	No connection
3	TRST_N	Host to Target	JTAG Test Reset - Active Low
4	GND	N/A	Ground
5	TDSRC	Host to Target	JTAG Test Data
6	XL1_UP1	Target to Host	XMOS Link
7	TMS	Host to Target	JTAG Test Mode Select
8	GND	N/A	Ground
9	TCK	Host to Target	JTAG Test Clock
10	XL1_UP0	Target to Host	XMOS Link
11	DEBUG	Bidirectional	Debug
12	GND	N/A	Ground
13	TDSNK	Target to Host	JTAG Test Data
14	XL1_DN0	Host to Target	XMOS Link
15	RST_N	Host to Target	System Reset - Active Low.
16	GND	N/A	Ground
17	UART_RX	Host to Target	Serial Port
18	XL1_DN1	Host to Target	XMOS Link
19	UART_TX	Target to Host	Serial Port
20	GND	N/A	Ground

The routing of these I/O pins along with the power pins is shown on the following page.



4.1 UART configuration

No UART hardware is provided. Instead, the UART is implemented in software by mapping the two UART pins to ports on the XS1-L device. The XTAG-2 performs a UART-to-USB conversion on these pins.



The table below shows the pin-to-port mapping.

Pin	Port		Processor
	1bit	4bit	
XD25	P1J0		UART_RX
XD26		P4E0	UART_TX

4.2 XMOS Link Configuration

Some of the I/O pins on the processor are configured as a duplex 2-bit serial XMOS Link. The mapping of XMOS Link to the pins is shown in the table below:

Pin	XMOS Link
XD4	XL1_UP1
XD5	XL1_UP0
XD6	XL1_DN0
XD7	XL1_DN1

4.3 JTAG Configuration

Some of the I/O pins on the processor are driven by the JTAG signals. The mapping of the signals to the pins is shown in the table below:

Pin	**Port**	**Processor**
XD0	P1A0	TDSRC
XD1	P1B0	TDSNK
XD10	P1C0	TMS
XD11	P1D0	TCK
XD35	P1L0	TRST_N

4.4 System Reset

The system reset signal is mapped to a 1-bit port on the processor as described below. It is used as an output to reset the target processor from the debugger

Pin	Port	Processor
XD36	P1IM	RST_N

5 13MHz Crystal Oscillator

The XS1-L1 is clocked at 13MHz by a crystal oscillator on the card. The processor is clocked at 400MHz and the I/O ports at 100MHz, by an on-chip phaselocked loop (PLL).

6 I/O Port-to-Pin Mapping

The table below provides a full description of the port-to-pin mappings described throughout this document.

Pin	Port			Processor
	1b	4b	8b	
X0D0	P1A0			TDSRC
X0D1	P1B0			TDSNK
X0D2		P4A0	P8A0	
X0D3		P4A1	P8A1	
X0D4		P4B0	P8A2	XL1_UP1
X0D5		P4B1	P8A3	XL1_UP0
X0D6		P4B2	P8A4	XL1_DN0
X0D7		P4B3	P8A5	XL1_DN1
X0D8		P4A2	P8A6	
X0D9		P4A3	P8A7	
X0D10	P1C0			TMS
X0D11	P1D0			TCK
X0D12	P1E0			ULPI_STP
X0D13	P1F0			ULPI_NXT
X0D14		P4C0	P8B0	ULPI_DATA[0:7]
X0D15		P4C1	P8B1	
X0D16		P4D0	P8B2	
X0D17		P4D1	P8B3	
X0D18		P4D2	P8B4	
X0D19		P4D3	P8B5	
X0D20		P4C2	P8B6	
X0D21		P4C3	P8B7	
X0D22	P1G0			ULPI_DIR
X0D23	P1H0			ULPI_CLK
X0D24	P1I0			PHY_RST_N
X0D25	P1J0			UART_RX
X0D26		P4E0		UART_TX
X0D27		P4E1		
X0D32		P4E2		
X0D33		P4E3		
X0D34	P1K0			DEBUG
X0D35	P1L0			TRST_N
X0D36	P1M0			RST_N
X0D37	P1N0			
X0D38	P1O0			
X0D39	P1P0			

Disclaimer

XMOS Ltd. is the owner or licensee of this design, code, or Information (collectively, the “Information”) and is providing it to you “AS IS” with no warranty of any kind, express or implied and shall have no liability in relation to its use. XMOS Ltd. makes no representation that the Information, or any particular implementation thereof, is or will be free from any claims of infringement and again, shall have no liability in relation to any such claims.